CDA 4203L Spring 2022

Computer System Design Lab

Lab 1 – Schematic Capture

*Handed out on Wednesday, 19th January*

*Due Date: 11:59 PM, Sunday, 30th January*

This is an individual assignment. No teaming allowed.

**Objectives:** To learn and practice schematic entry and simulation.

**Problem:** Implement an ALU (Arithmetic Logic Unit) satisfying the following functional requirements. You should complete schematic capture tutorial, before you start on this lab.

|  |  |  |
| --- | --- | --- |
| Function | Select (S)  S1 S0 | Y |
| Invert | 0 0 |  |
| Add | 0 1 | A + B |
| Subtract | 1 0 | A - B |
| Double | 1 1 | 2\*A |

A

**A L U**

Y

S

4

2

4

B

4

Figure 1: ALU Port Interface and Function Table

1. (10 pts) Design and create a schematic of the ALU using ISE Schematic Entry tool.
2. (10 pts) Create a test bench and use it to test the ALU functionality. Include at least two test vectors per function.

**Deliverables:** A concise report that includes your design and simulation results.

**Report Organization (A template will be provided on Canvas):**

* Cover sheet
* ALU schematic
* Brief description of your design
* Simulation waveforms
* IP Block
* Feedback: Hours spent, Exercise difficulty (Easy, Medium, Hard)

**Important:**

* Do not discard your design. It will be used as starting point for subsequent lab exercise(s).
* You need to submit your report on Canvas in PDF format. No hardcopy is needed.